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LMS adaptive loop module

Abstract:

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An apparatus for cancelling undesired signals received with a desired signal. The received signals (1) are supplied to a first hybrid (2) which provides reference (3) and auxiliary (4) signals. The auxiliary (4) signal is provided to a second hybrid (16) which provides in-phase (17) and quadrature (18) signals which are weighted in mixers (19, 20) by drive signals via lines (14, 15) from an adaptive loop including correlator multipliers (10) and a loop controller (13). The weighted in-phase (21) and quadrature (22) signals and the reference (3) signal are summed in a summer 9 to provide an output signal (8). The adaptive weighting is provided by correlating a signal from a coupler (5) connected to auxiliary signal port (4) with a feedback signal via a line (7) from the apparatus output (8), in the correlator 10. The adaptive loop is controlled by a single monolithic NMOS device in controller (13) having in-phase and quadrature baseband processors.

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(54) LMS adaptive loop module

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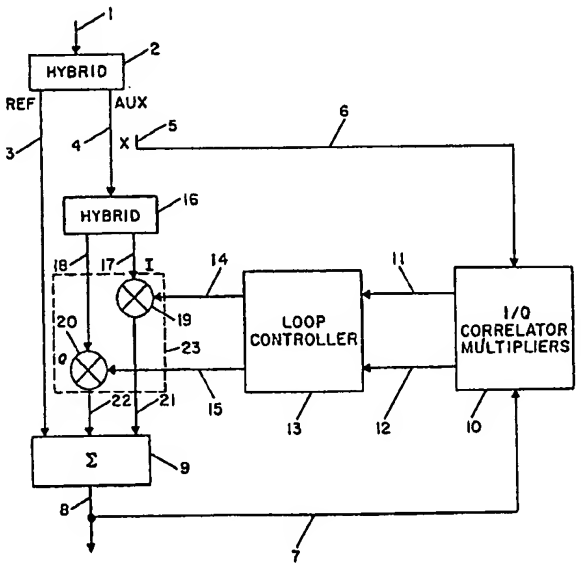

FIG. 1

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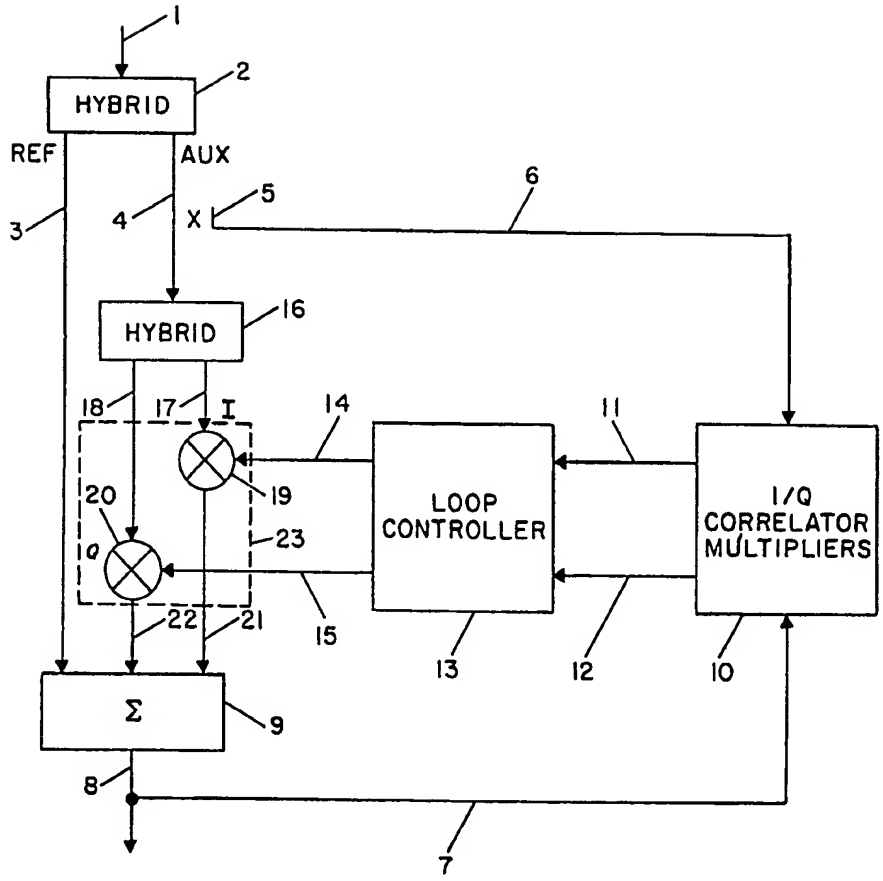
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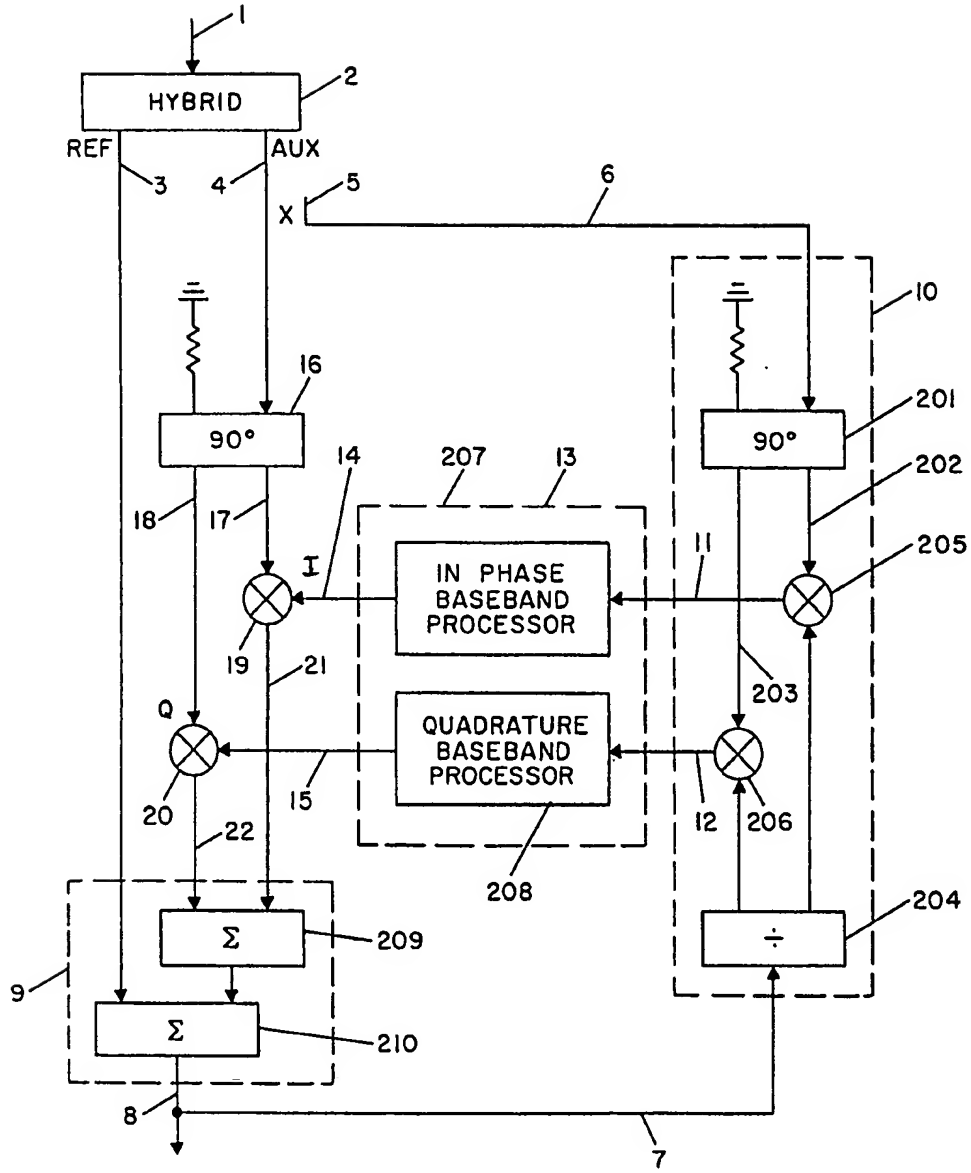
HYBRID
2
REF
AUX
3
4
X
5
6
HYBRID
16
18
17
I
14
11
20
19
Q
23
LOOP CONTROLLER
I/Q CORRELATOR MULTIPLIERS
22
21
15
13
12
10
Σ
9
8
7

FIG. 1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REF
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4
5
X
6
10
16
90°
201
90°
14
207
13
202
18
17
I
IN PHASE
BASEBAND
PROCESSOR
11
205
19
21
203
Q
QUADRATURE
BASEBAND
PROCESSOR
20
15
12
206
22
208
204
Σ
209
÷
9
Σ
210
8
7

FIG. 2

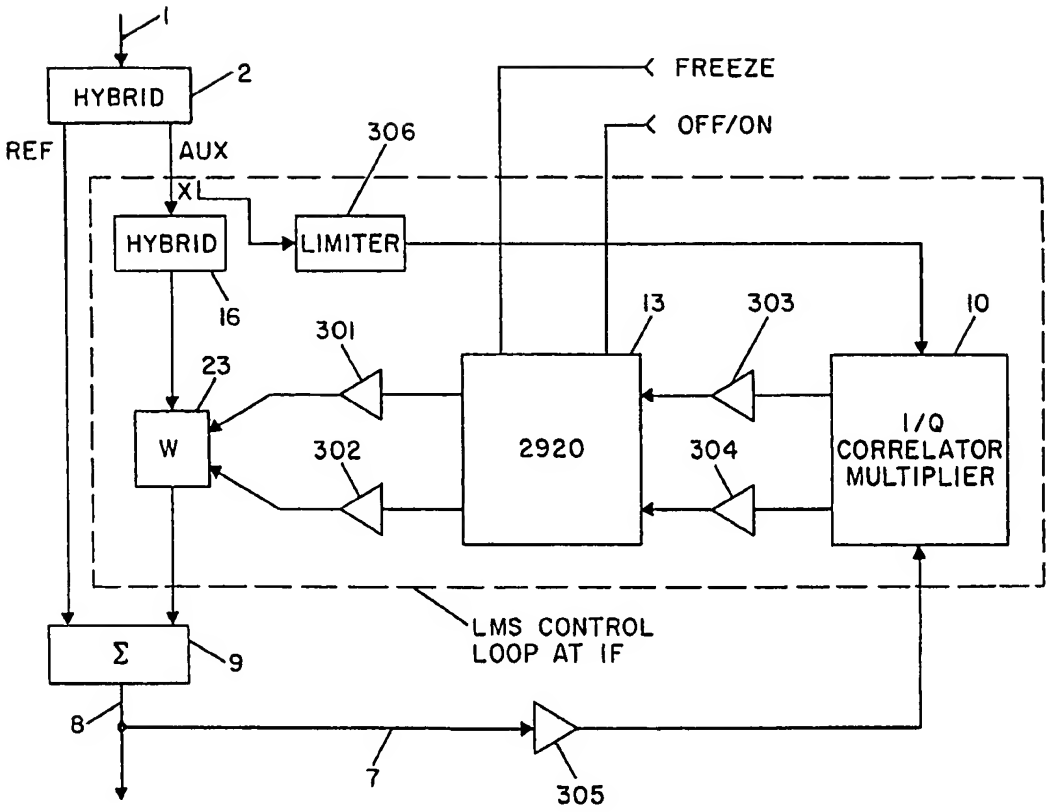
1
HYBRID
2
REF
AUX
306
FREEZE
OFF/ON
X
HYBRID
LIMITER
16
13
303
10
301
23
W
302
2920
304
I/Q
CORRELATOR
MULTIPLIER
LMS CONTROL
LOOP AT IF
Σ
9
8
7
305

FIG. 3

SPECIFICATION

LMS adaptive loop module

The invention relates generally to adaptive control loops for reducing the effects of received interference and, in particular, to a low cost LMS loop module.

Many current and planned communications, radar, avionics and microwave systems use LMS (least mean square) adaptive control loops to reduce the effects of received interference. Although most applications have addressed adaptive spacial processing, LMS techniques have been used in the time, frequency and polarization domains. Systems have been studied potentially requiring tens to hundreds of individual control loops. These systems range in operational radio frequency carrier frequencies from VLF to EHF. Channel bandwidths can vary from tens to hundreds of hertz to hundreds of megahertz. Desired signal modulations cover virtually all known formats. As the potential for large scale production of many LMS-equipped systems increases, there is a need for a common low cost LMS loop module employing advanced single chip, signal processing devices such as Intels's 2920, NEC's uPD 7720, TI's TMS320 and the S2811 manufactured by American Micro Systems, Inc.

It is an object of this invention to provide a small, low cost adaptive control loop module using the LMS alogorithm in order to make sophisicated ECCM processors economically feasible while maintaining high performance.

It is another object of this invention to provide a loop module which is compatible with many current and future communications systems by virtue of a design which can be implemented using advanced microcircuit technology.

The apparatus according to the invention is for cancelling undesired signals received with a desired signal. The apparatus has an output port and provides an output signal. First means provides the desired signal and any undesired signals received with the desired signal. A first hybrid has an input port coupled to the first means and has a reference output port and an auxiliary output port. The second hybrid has an input port coupled to the auxiliary output port and provides an in-phase output signal and a quadrature output signal. A first input port of an in-phase correlator multiplier is coupled to the auxiliary output port. The multiplier has a feedback input port coupled to the apparatus output port and provides an output signal. A first input port of a quadrature correlator multiplier is coupled to the auxiliary output port. The quadrature correlator multiplier has a feedback input port coupled to the apparatus output port and provides an output signal. The apparatus further includes means for providing in-phase drive signals and quadrature drive signals corresponding to the output signals of the in-phase and quadrature correlation multipliers, respectively. Means are provided for weighting the in-phase and quadrature output signals provided by the second circuit as it responds to the in-phase and quadrature drive signals. Means for summing the weighted in-phase and quadrature output signals and the signals provided by the referenced output ports is provided, said means for summing having the apparatus output port.

For a better understanding of the present invention, together with other and further objects, reference is made to the following description, taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appended claims.

Figure 1 is a functional block diagram of an LMS loop module according to the invention.

Figure 2 is a functional block diagram of the module of Figure 1 specifically illustrating the multiplier and controller functions.

Figure 3 is a detailed block diagram of a low cost LMS loop module according to the invention including a single-chip signal processing device.

Figure 1 illustrates a module according to the invention. An incoming or received signal 1 including desired and undesired signals is provided to hybrid 2 which generates a reference signal at reference port 3 and an auxiliary signal at auxiliary port 4. Reference port 3 emulates the protected antenna in an adaptive spacial processor while auxiliary port 4 emulates other suitably derived antenna signals. The purpose of the module is to reduce the power of the interfering signal by weighting the auxiliary signal.

Coupler 5 is connected to auxiliary port 4 and provides a reference branch signal via line 6 which is correlated with a feedback signal provided via line 7. The feedback signal is derived from the output 8 provided by summer 9. The correlation process is conveniently separated into the functions of multiplication and baseband integration as discussed below. I/Q correlator multipliers 10 generate I and Q baseband signals via lines 11 and 12 which are processed by loop controller 13 to generate in-phase drive signals via line 14 and quadrature drive signals via line 15 for driving the complex weighting of the auxiliary signal.

Such weighting of the auxiliary signal provided by the auxiliary port of hybrid 2 is accomplished in the following manner. The auxiliary signal is supplied to hybrid 16 which provides an in-phase signal at in-phase port 17 and a quadrature signal at quadrature port 18. The in-phase signal is weighted by mixer 19 driven by the in-phase drive signal provided via line 14. Similarly, the quadrature auxiliary signal is weighted by mixer 20 which is driven by quadrature drive signals provided by line 15. The weighted auxiliary signals provided by the outputs 21 and 22 of the mixers are summed by summer 9 with the referenced signal provided by reference port 3 to reduce the power of the interfering signals. The resulting signal provided by output 8, as compared to the incoming signal provided to input 1, has a higher desired signal-to-noise ratio.

The essential functions of the LMS control loop according to the invention include: (a) a complex (phase-amplitude) weighting provided by mixers

19 and 20; (b) correlation multiplication provided by I/Q correlation multiplier 10; (c) auxiliary reference branch processing via line 6 used to recondition one input to correlation multiplier 10; (d) a common feedback branch provided via line 7; and (e) a flexible baseband signal processor i.e. loop controller 13. Required capability, particularly with respect to bandwidth, is maximized by adapting a hybrid analog/digital approach in which functions (a) through (d) are implemented with analog circuits while function (e) is implemented with a hybrid device in the form of loop controller 13. As a result, the approach is applicable to any IF frequency depending in implementation tradeoffs or functions (a) through (d).

As shown in Figure 2, I/Q correlator multiplier 10 may be implemented by I/Q hybrid 201 providing an in-phase signal corresponding to the auxiliary signal via line 202 and a corresponding quadrature signal via line 203. These signals are mixed with the feedback signal provided by divider 204 by mixers 205 and 206 to complete the multiplication function and generate I and Q baseband signals via lines 11 and 12 which are provided to loop controller 13.

Controller 13 includes in-phase baseband processor 207 and quadrature baseband processor 208 which generate in-phase drive signals provided by line 14 and quadrature drive signals provided by line 15. These drive signals drive mixers 19 and 20 providing output signals via lines 21 and 22 which are summed by summer 209 and provided to summer 210 for addition with the reference signal provided by reference port 3.

As illustrated by Figure 3, the Intel 2920 may be used as loop controller 13. The Intel 2920 is a signal processor chip combining alalog functional elements with a digital processing capability in a single monolithic device. The device is fabricated with VLSI technology using an NMOS process.Preferably, the 2920 chip is programmed to provide a digital filter having a 1hz bandwith for both I and Q channels with a baseband gain of 36dB. An additional gain of 23dB may be achieved by operational amplifiers 301 and 302. Furthermore, the chip may be programmed to provide a weight freeze function and an off/on function. Operational amplifiers 303 and 304 may be used to interface the I/Q correlator multiplier 10 with the loop module 13. Commonality is achieved by designing the module at a standard IF frequency of 70Mhz. In order to accommodate wide bandwidths, the weighting network and correlator multiplier are analog and may be implemented with thick film technology. Use of the Intel 2920 is possible because loop controller 13 does not necessarily require a sampling speed equal to that of the Nyquist rate for broad band systems. Controller bandwidth requirements are principally dictated by platform jammer dynamics in many system applications. Convergence or transient response is inversely proportional to the baseband controller sampling rate. Since the loop controller provides integration and baseband gain in both the I and Q paths it can easily be implemented digitally using current LSI technology for systems which do not require an extremely fast convergence time.

A loop module according to the invention as illustrated in Figure 3 was tested with both CW and broadband noise jamming signals. Results of this testing showed a significant cancellation on CW over a 20-Mhz bandwidth for a noise jammer. The results of such testing show that the requirements of many adaptive antenna systems can be met using current LSI technology at low cost and a package that is 4.3cm X 4.3cm x 0.5cm. The convergence time is adequate to track aircraft dynamics by many airborne systems. Limiter 306 preconditions the auxiliary input of I/Q correlator multiplier 10 and IF amplifier 305 is used in line 7 to control the amplitude of the feedback signal being supplied to multiplier 10.

CLAIMS

1. An apparatus for cancelling undesired signals received with a desired signal and having an output port for providing an output signal, said apparatus comprising:

a. First apparatus for providing the desired signal and any undesired signal received with the desired signal;

b. A first hybrid having an input port coupled to said first apparatus and having a reference output port and an auxiliary output port;

c. A second hybrid having an input port coupled to the auxiliary output port and providing an in-phase output signal and a quadrature output signal;

d. An in-phase correlator multiplier having a first input port coupled to the auxiliary output port and a feedback input port coupled to the apparatus output port, said in-phase correlator multiplier providing an output signal;

e. A quadrature correlator multiplier having a first input port coupled to the auxiliary output port and a feed back input port and a feedback input port coupled to the apparatus output port, said quadrature correlator multiplier providing an output signal;

f. Second apparatus for providing an in-phase drive signal and a quadrature drive signal corresponding to the output signals of the in-phase and quadrature correlator multipliers, respectively;

g. Third apparatus for weighting the in-phase and quadrature output signals provided by the second hybrid in response to the in-phase and quadrature drive signals, respectively; and

h. A summing apparatus for summing the weighted in-phase and quadrature output signals and signals provided at the reference output port, said means for summing having the apparatus output port.

2. The apparatus of claim 1 wherein said second apparatus for providing in-phase and quadrature drive signals comprises an in-phase baseband processor and a quadrature baseband processor.

3. The apparatus of claim 2 wherein said baseband processors comprise a single monolithic NMOS device.